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Embedded Memory Technologies –
the First Step Towards SoC

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Over the last four decades, the semiconductor industry has created four basic types of product classes which are identified also as sub-systems: MPU (which is representative for logic), ASIC/FPGA (for field programmability), DRAM (for memories) and AMS (for analog/mixed signal). The need to continuously improve these product classes has lead to optimized sub-system performance and cost to the detriment of system performance and cost.

Forecasted developments in the computer, communications and consumer markets however, will require electronic systems with significantly improved performance and cost characteristics. The "Moore business plan," which has driven the semiconductor industry for four decades, needs to be amended, updated and complemented in order to guide the industry in the future. The new version has been dubbed "SoC business plan."

According to the "SoC business plan" the mature product classes will become obsolete not from a technology perspective, but from an economic perspective. They will be "morphed" into advanced product classes, SoC (system-on-chip) and SiP (system-on-package), which will have as overriding objective a step increase in performance and cost on system level, rather than on sub-system level.

The "morphing" process of the mature product classes into advanced product classes will be a gradual process which will require significant design and manufacturing technology developments. This process represents a paradigm change for the entire semiconductor industry, as the focus shifts from sub-system to system optimization. The first step will be the gradual harmonization of MPU (logic) and ASIC with memory technologies, into "embedded memory" configurations.

The presentation will put in perspective the transition from the mature product classes to "embedded memories" and to SoC. It will focus on the challenges and requirements of integrating different NVM technologies with logic. In addition, it will contrast the market requirements for embedded memory configurations with the technical and especially economic limitations.